Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	N/A
Filing Date	Herewith
First Named Inventor:	Zorian
Art Unit	N/A
Examiner Name	Unassigned
Attorney Docket Number	04640.P019

Sheet	1	of	2

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JK		US-	5,513,318	04/30/1996	Van de Goor, et al.	
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		US-				
		US-				
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	/James Kerveros/	Date Considered	08/31/2006

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/James Kerveros/

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				Art Unit	N/A
				Examiner Name	Unassigned
Sheet	2	**of**	2	Attorney Docket Number	04640.P019

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
JK		Yervant Zorian: "System-Chip Test Strategies" (Tutorial): DAC 1998: 752-757.	
		Ilyoung Kim, Yervant Zorian, Goh Komoriya, Hai Pham, Frank P. Higgins, Jim L. Lewandowski: " Built-in Self-Repair for Embedded High Density SRAM." ITC 1998: 1112-1119	
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		Yervant Zorian, Erik Jan Marinissen, "System Chip Test: How Will It Impact Your Design?", DAC, 2000, pages 1-6.	
		Monica Lobetti Bodoni, Alfredo Benso, Silvia Chiusano, Stefano DiCarlo, Giorgio DiNatale, Paolo Prinetto, "An Effective Distributed BIST Architecture for RAMs," pages 1-6, IEEE European Test Workshop, 2000.	
		Chauchin Su, Shih-Ching Hsiao, Hau-Zen Zhau, Chung-Len Lee, "A Computer Aided Engineering System for Memory BIST,", DAC, 2001 pages 1-4.	
		Yervant Zorian, "Embedding Infrastructure IP for SOC Yield Improvement," , June 2002, 709-712.	
		Praveen Parvathala, Kailas Maneparambil, William Lindsay, "FRITS – A Microprocessor Functional BIST Method," ITC, Mar. 2002, pages 590-598.	
		TechWeb definition, AUTHOR UNKNOWN, scan technology, copyright 1981-2001, 1 page.	
		S. Shoukourian, V. Vardanian, Y. Zorian, "An Approach for Evaluation of Redundancy Analysis Algorithms," The Proceedings of IEEE Int. Workshop on Memory Technology, Design and Testing, 2001.	
		D.K. Bhavsar, "An Algorithm for Row-Column Self-Repair of RAMs and its Implementation in the Alpha 21264," Proc. ITC'1999, pp. 311-318.	
		T. Kawagoe, J. Ohtani, M. Niiro, T. Ooishi, M. Hamada, H. Hidaka, "A Built-In Self-Repair Analyzer (CRESTA) for Embedded DRAMs," Proc. ITC'2000, pp. 567-574.	

Examiner Signature	/James Kerveros/	Date Considered	08/31/2006

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